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(54) **A DEDICATED INTERFACE ARCHITECTURE FOR A HYBRID CIRCUIT**

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## Description

**[0001]** The present invention relates to a hybrid integrated circuit containing an FPGA portion and an ASIC portion. More particularly, this invention relates to an interface between the FPGA and the ASIC portions of a hybrid integrated circuit.

**[0002]** A field programmable gate array (FPGA) may be programmed to execute a wide variety of logic functions, providing designers the ability to design circuits for specific applications. Other advantages of an FPGA are that the design time is short so it can be marketed much quicker and the design is such that can be changed easily. In an FPGA, however, many of the gates may go unused. An application-specific integrated circuit (ASIC), on the other hand, is designed only to perform certain specific tasks, and therefore does not result in wasted gates. However the design and testing phase of an ASIC is quite complex and expensive because an ASIC must be mask-programmed, and therefore the production of an ASIC only makes fiscal sense when the ASIC is to be produced in large quantities.

**[0003]** A hybrid integrated circuit (IC) provides some portion of the advantages of both designs. A hybrid IC includes both an FPGA and an ASIC portion. Of major concern in designing a hybrid IC is providing a suitable interface between the FPGA and ASIC portions of the IC. In order for the IC to perform its tasks properly, the FPGA and ASIC portions must be able to communicate effectively with each other. Conventionally, the interface has been designed to have the ASIC portion communicate with the FPGA portion, as will be described below, through the boundary between the FPGA portion and the ASIC portion using a plurality of connections between the edge of the ASIC portion and the edge of the FPGA portion.

**[0004]** FIGS. 1A-1F depict several examples of different designs of the layout architecture of a hybrid IC as known in the art. In FIGS. 1A-1F, each IC 2 has a plurality of I/O modules 10 running along the perimeter of the IC 2 wherein the orientation of the FPGA portion 14 and the ASIC portion 12 varies among the figures.

**[0005]** FIG. 1A illustrates a smaller ASIC portion 12 positioned below a larger FPGA portion 14. FIG. 1B illustrates a larger ASIC 12 portion positioned below a smaller FPGA 14 portion. FIG. 1C illustrates an ASIC portion 12 positioned at the bottom right corner of an FPGA portion 14. FIG. 1D illustrates an ASIC portion 12 positioned at the upper left corner of and FPGA portion 14. FIG. 1E illustrates an ASIC portion 12 positioned within an FPGA portion 14, near the bottom right corner. FIG. 1F illustrates an FPGA portion 14 positioned within an ASIC portion 12, near the upper left corner. It will be appreciated that other orientations of the FPGA portion 14 and the ASIC portion 12 of the IC 2 are well known in the art.

**[0006]** In FIG. 2, the FPGA portion 14 and the ASIC portion 12 of the IC 2 depicted in FIG. 1A are illustrated

in greater detail. In FIG. 2, the FPGA portion 14 is made up of an array of logic modules 16 with horizontal and vertical routing resources provided for connecting the logic modules 16 as well as for communication with the ASIC portion 12. Communication between the ASIC portion 12 and the FPGA portion 14 is then accomplished by connecting the ASIC portion 12 to the boundary between the FPGA portion 14 and the ASIC portion 12. The boundary between the FPGA portion 14 and the ASIC portion 12 is connected to the vertical or horizontal routing resources. Signals are then sent from the ASIC portion 12 through the boundary between the ASIC portion 12 and the FPGA portion 14 and through the horizontal and vertical routing resources until reaching the desired logic modules 16. Communication from the logic modules 16 of the FPGA portion 14 to the ASIC portion 12 is accomplished in the reverse manner by sending signals from the desired logic modules 16 through the horizontal and vertical routing resources of the FPGA portion 14 until reaching the boundary between the FPGA portion 14 and the ASIC portion 12 and into the ASIC portion 12.

**[0007]** FIG. 3 depicts another embodiment of a hybrid IC as known in the art. This embodiment contains an FPGA portion 14 having a multi-level hierarchical design (in this example, a three-level hierarchical design) rather than simply an array of logic modules. The FPGA portion 14 comprises nine logic blocks 18 having horizontal and vertical routing resources. Each logic block 18 comprises another nine logic blocks 20 having local routing resources. The logic blocks in the second level of the hierarchical design will be termed clusters in this specification to distinguish them from the logic blocks in the first level of the hierarchical design. It should be appreciated, however, that since such a hierarchical design may conceivably have an unlimited number of levels, each having logic blocks and local routing resources, the term "cluster" should not be read as limiting the invention to only a three-level design. Each of the logic blocks (clusters) 20 then comprises a plurality of logic blocks, which in this example are logic modules with local routing resources, but may also be configurable function generators, logic blocks containing another level of logic blocks, etc.

**[0008]** Communication between the ASIC portion 12 and the FPGA portion 14 is accomplished by connecting the ASIC portion 12 to the boundary between the FPGA portion 14 and the ASIC portion 12 and the first level of horizontal or vertical routing resources to the boundary between the FPGA portion 14 and the ASIC portion 12. Signals are then sent from the ASIC portion 12 through the boundary between the FPGA portion 14 and the ASIC portion 12 and through the horizontal and vertical routing resources at the first hierarchical level (the routing resources positioned between each logic block 18). The signals then pass to the horizontal and vertical routing resources at the second hierarchical level (the routing resources between each logic block or cluster 20) and

then the third hierarchical level (the routing resources between each logic block at this level).

**[0009]** The interfaces described have several drawbacks. First, these interfaces run at relatively slow speeds. This slow speed is exasperated by the relatively large distances between the logic modules and the interface. Second, routing congestion is common at the boundary between the FPGA portion 14 and the ASIC portion 12 in these types of designs. Alleviating this routing congestion using a routing resource requires that a significant amount of space be allocated for the routing resource between the FPGA portion 14 and the ASIC portion 12.

**[0010]** In addition to the routing and speed problems of the prior art interfaces, the fixed pin location and order for signals sent from the ASIC 12 portion to the FPGA 14 portion may cause FPGA place and route difficulties. Also, the asymmetrical number of I/O connections required for each side of the FPGA portion may also cause FPGA place and route difficulties.

**[0011]** Another drawback of these interfaces is that they require that both the FPGA portion 14 and the ASIC 12 portion be hardwired onto the IC 2 during the design phase. This prevents the use of interchangeable modules for the FPGA portion 14 and the ASIC portion 12.

**[0012]** Clearly, an interface between the FPGA and ASIC portions of a hybrid IC that does not suffer from the drawbacks of the prior art is needed.

**[0013]** WO 98/13938 discloses a heterogeneous IC device comprising an FPGA connected to a mask-designed application specific logic area. Routing of signals is implemented as a combination of mask-designed and field programmable interconnections.

**[0014]** The present invention provides an interface architecture as defined in the appended claims. The interface design for a hybrid IC utilizes dedicated interface tracks to allow signals to interface distributively with the logic blocks of the FPGA portion providing for faster and more efficient communication between the FPGA and ASIC portions of the hybrid IC.

**[0015]** According to a first embodiment of the present invention, a plurality of dedicated interface tracks are connected directly between the ASIC portion and each individual logic block at the lowest level of the FPGA portion of a hybrid IC. By providing a direct connection from the ASIC portion to individual logic blocks of the FPGA portion, the local routing resources may be bypassed. As a result, there is less congestion in the system.

**[0016]** According to a second aspect of the present invention, the dedicated interface tracks are connected directly between the ASIC portion to logic blocks at any level of the FPGA portion of a hybrid IC. Connection to the lowest level of logic blocks is accomplished using local routing resources. This design has the advantage of bypassing some of the local routing resources, easing congestion and increasing speed, but allowing some local routing resources to complete the connection to the logic blocks at the lowest level of the FPGA portion of

the hybrid IC.

## BRIEF DESCRIPTION OF THE DRAWINGS

5 **[0017]**

FIGS. 1A-1F illustrate various placements of the ASIC portion and FPGA portion of a hybrid IC as known previously in the art.

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FIG. 2 illustrates a first embodiment known in the art of the arrangement of logic modules and their connection to an ASIC portion of a hybrid IC.

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FIG. 3 illustrates a second embodiment known in the art of the arrangement of logic modules and their connection to an ASIC portion of a hybrid IC.

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FIG. 4 illustrates a general view of a preferred embodiment according to the present invention.

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FIG. 5 illustrates in greater detail the embodiment in FIG. 4, indicating the internal workings of the FPGA-ASIC routing channel, the interface buffers, and the direct interface tracks.

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FIG. 6 illustrates in greater detail the embodiment in FIG. 4, indicating how the direct interface tracks connect to the logic modules or local or global routing resources.

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FIG. 7 illustrates another embodiment of the present invention, indicating the addition of JTAG or other diagnostic buffers to the connection between the ASIC portion and the FPGA portion of the hybrid IC.

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FIG. 8 illustrates in greater detail the embodiment in FIG. 7, indicating the internal workings of the FPGA-ASIC routing channel, the interface buffers, the JTAG buffers, and the direct interface tracks.

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FIG. 9 illustrates another embodiment of the present invention, indicating how the I/O modules may be directly interfaced with the FPGA through the interface between the FPGA portion and the ASIC portion.

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FIG. 10 illustrates another embodiment of the present invention, indicating how the interface may be expanded to two sides of the IC.

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FIG. 11 illustrates another embodiment of the present invention, indicating how the ASIC portion may be connected directly to the interface buffers, without passing through a programmable routing channel.

FIG. 12 illustrates another embodiment of the present invention, indicating that the ASIC portion may be connected directly to the FPGA portion, without passing through a programmable routing channel or interface buffers.

FIG. 13 illustrates another embodiment of the present invention, indicating that the I/O modules or interface buffers may be located inside the individual components.

FIG. 14 illustrates another embodiment of the present invention, indicating that the I/O modules or interface buffers may be located inside the individual components, residing only in the bottom row of components.

#### DETAILED DESCRIPTION OF THE INVENTION

**[0018]** Those of ordinary skill in the art will realize that the following description of the present invention is illustrative only and not in any way limiting. Other embodiments of the invention will readily suggest themselves to such skilled persons.

**[0019]** According to a first embodiment of the present invention, a plurality of dedicated interface tracks are connected directly between the ASIC portion and each individual logic block at the lowest level of the FPGA portion of a hybrid IC. By providing a direct connection from the ASIC portion to individual logic blocks of the FPGA portion, the local routing resources may be bypassed. As a result, there is less congestion in the system.

**[0020]** According to a second aspect of the present invention, the dedicated interface tracks are connected directly between the ASIC portion to logic blocks at any level of the FPGA portion of a hybrid IC. This design has the advantage of bypassing some of the local routing resources, easing congestion and increasing speed, but allowing some local routing resources to complete the connection to the logic blocks at the lowest level of the FPGA portion of the hybrid IC.

**[0021]** One of ordinary skill in the art will recognize that the FPGA portion may have a hierarchical design made up of any number of levels, each level containing one or more blocks, each block possibly containing another level of blocks or, at the lowest level of the design, a logic module, configurable function generator, etc. Each level in the hierarchical design may then also contain local routing resources, allowing communication between each block but also allowing communication to a dedicated interface track if the designer so wishes.

**[0022]** A hierarchical FPGA architecture is depicted in FIG. 4 similar to that described above with respect to FIG. 3. Briefly, the hierarchical FPGA architecture has various horizontal and vertical interconnect conductors that programmably connect groups of logic resources at each level in the hierarchical design. FIG. 4 further illustrates a hybrid IC 2 architecture having dedicated inter-

face tracks 24 connected between the ASIC portion 12 and each logic block 20 at the lowest level of the FPGA portion 14. The invention is not limited to direct connection to the logic blocks 20 in the hierarchical design of FIG. 4, but may also be employed to connect directly to the logic blocks at any level of the FPGA portion 14 of any hybrid IC. In an alternative embodiment, the dedicated interface tracks 24 may be connected to the local interconnect conductors between the logic blocks 20 of an FPGA portion of a hybrid IC. This may be accomplished by connecting the dedicated interface tracks 24 to the local interconnect conductors at the edge of a block 22 located on a higher level.

**[0023]** In FIG. 4, interface buffers 26 and a routing channel 28 are placed between the FPGA portions and the ASIC portion. The dedicated interface tracks 24 run from the individual components to the interface buffers 26. The interface buffers 26 are connected to the routing channel 28, which is then connected to the ASIC portion 12. Thus a signal from the ASIC portion 12 passes through the routing channel 28, then through the interface buffers 26, then to the dedicated interface tracks which complete the connection to individual logic modules. The interface buffers 26 and the routing channel 28 are, however, optional devices and are not required for the use of the present invention.

**[0024]** FIG. 5 depicts the interface buffers 26 and the FPGA-ASIC routing channel 28 of FIG. 4 in greater detail. Each interface buffer 26 may include an output buffer 30, an input buffer 32, first, second, and third multiplexors 34-1, 34-2, and 34-3, a configurable register, memory, or programmable elements 36, and may also contain a first and second local enable 38-1 and 38-2. The first and second local enables 38-1 and 38-2 may be connected to programming elements in the FPGA-ASIC routing channel 28. The interface buffer 26, however, is not limited to this design and may be any type of buffering or logic device that performs buffering. Therefore, signals to be sent from the ASIC portion 12 to the FPGA portion 14 may first travel through the FPGA-ASIC routing channel 28, which directs them to the appropriate local enables 38, which in turn travel through the interface buffer 26 to the appropriate inbound dedicated interface track leading to a logic block in the FPGA portion 14. Should the same signals need to be sent to a plurality of logic blocks of an FPGA portion 14 at the same time, global enables 40, which connect to all of the interface buffers in the same way that the local enables 38 connect to single interface buffers, may be used.

**[0025]** Signals from the FPGA portion 14 to the ASIC portion 12 are handled in the reverse direction. One interesting result of the design of the interface buffers depicted in FIG. 5 is the ability of the interface buffers to route the output of the FPGA portion 14 back into the FPGA portion 14 without first going through the FPGA-ASIC routing channel 28 or through the ASIC 14 itself. This allows for more flexibility in the design and pro-

gramming of these integrated circuits, as communication between elements of the FPGA portion 14 may be facilitated without the use of routing resources within the FPGA portion 14 itself.

**[0026]** The FPGA-ASIC routing channel 28 depicted in FIG. 5 may be either hardwired or contain a plurality of programming elements 42. These programming elements may be elements like an SRAM, an antifuse, and an EPROM, for example. This routing resource is employed to facilitate the distribution of the signals between the ASIC portion 12 and the FPGA portion 14. It will be appreciated by those of ordinary skill in the art that there are many ways to accomplish this distribution of signals, only one of which is through an FPGA-ASIC routing channel 28.

**[0027]** FIG. 6 illustrates in greater detail the connections between the dedicated interface tracks and the individual blocks or modules, or local or global routing resources of the FPGA portion 14 of the hybrid FPGA-ASIC 2 of FIG. 4. In FIG. 6, logic modules are depicted as the blocks 44 at the lowest level of the FPGA portion 14. However, those of ordinary skill in the art will recognize that any number of different types of modules may be placed at the lowest level of an FPGA portion 14. FIG. 6 depicts three of the many different ways in which the dedicated interface tracks 24 may be connected. Junction 46 shows a dedicated interface track 24 hardwired to a block (cluster) 20 in the second level of the hierarchical design. Junction 48 shows a dedicated interface track 24 connected to a block (cluster) 20 in the second level of the hierarchical design through the use of a programmable element. In the blocks 20 connected to each of junctions 46 and 48, local routing resources within the block 20 will have to complete the connected between the dedicated interface tracks 24 and the logic block 44 at the lowest level of the design. Junction 50 depicts a dedicated interface track 24 connected directly to a block 44 at the lowest level of the FPGA portion 14.

**[0028]** Connecting the dedicated interface tracks directly to each block 44 at the lowest level of the FPGA portion 14 results in less congestion and, therefore, higher speed communications through the integrated circuit. However, connection directly to each block 44 at the lowest level of the FPGA portion 14 requires a large number of direct interface tracks 24. Therefore, it may be desirable to connect a portion or all of the dedicated interface tracks 24 to blocks at a higher level of the hierarchical design and allow local routing resources to complete the connection. This will reduce the number of dedicated interface tracks 24 required on the IC. While this will also reduce the speed of the communications, it is still faster than the prior art interfaces and it avoids the routing congestion at the FPGA-ASIC boundary that occurs in the prior art.

**[0029]** In an alternative embodiment illustrated in FIG. 7, a JTAG or other diagnostic 52 feature is depicted having a plurality of JTAG or diagnostic buffers 54. This fea-

ture is useful in testing the hybrid IC 2.

**[0030]** FIG. 8 depicts the bottom of an IC containing such a JTAG or other diagnostic feature 52 as illustrated in FIG. 7 in greater detail. One of ordinary skill in the art will recognize that the JTAG or other diagnostic feature 52 is only one way to test a hybrid IC, and it may be implemented in many possible ways, only one of which is depicted in the figures.

**[0031]** In another alternative embodiment illustrated in FIG. 9, I/O modules 10 which had, in previous figures, been attached directly to the ASIC portion 12, may instead be directly interfaced with the FPGA 14, either with or without the JTAG or other diagnostic feature 52, the FPGA-ASIC routing channel 28, and the interface buffers 26. Additionally, I/O modules 10 may be connected directly to the FPGA-ASIC routing channel 28 or to the JTAG or other diagnostic buffers 52. Individual I/O modules may also be connected to more than one device, providing input or output to multiple devices simultaneously.

**[0032]** In FIG. 10, according to the present invention, a second side 72 of the hybrid IC is illustrated. Dedicated interface tracks from the second side 72 may either directly interface with the logic blocks of the FPGA portion 14 or interface with the dedicated interface tracks of the first side using programmable elements or the like. Those of ordinary skill in the art will recognize that there are many possible ways to connect the dedicated interface tracks of the second side 72 to either the FPGA portion 14 or the dedicated interface tracks of the first side. It is also clear that the present invention may similarly be expanded to a three or a four-sided embodiment.

**[0033]** FIG. 11 depicts an example of a hybrid IC 2 that utilizes interface buffers 26 but not an FPGA-ASIC routing channel. FIG. 12 depicts an example of a hybrid IC 2 that does not utilize either interface buffers or a FPGA-ASIC routing channel, but instead connects the ASIC portion 12 directly to the FPGA portion 14 through the dedicated interface tracks.

**[0034]** FIG. 13 illustrates another way to place interface buffers or I/O modules on the hybrid FPGA-ASIC. An input/output module (IOM) 82 or an interface buffer 84 may be placed inside the logic blocks in the FPGA portion should the designer so desire. FIG. 14 depicts a design similar to that of FIG. 13, except where each IOM 82 and interface buffer 84 is placed in the bottom row of blocks or clusters in order to reduce the length of the dedicated interface tracks that connect them to the ASIC portion.

## Claims

1. An interface architecture in an integrated circuit comprising:

an FPGA portion (14) of said integrated circuit

having logic blocks (20) for implementing logic functions and interconnect connectors for programmably connecting said logic blocks; an ASIC portion (12) of said integrated circuit having mask programmed logic circuits and mask programmed interconnect conductors between said logic circuits; mask programmed dedicated interface tracks (24) connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion; and interface buffers disposed in series with said dedicated interface tracks between said FPGA portion and said ASIC portion;

**characterised in that:**

each of said interface buffers includes:

an input buffer (32),  
an output buffer (30), said output buffer connected to said input buffer;  
three multiplexors, two of said multiplexors (34-1, 34-2) connected to said output buffer and one of said multiplexors (34-3) connected to said input buffer; and  
a configurable register, memory store or programmable element (36) connected to each set of said multiplexors.

2. The interface architecture of claim 1, wherein the interconnect conductors in said FPGA portion include local routing resources.
3. The interface architecture of claim 1, further including an FPGA-ASIC routing channel arranged between said dedicated interface tracks and said ASIC portion.
4. The interface architecture of claim 1, wherein said FPGA portion has a hierarchal design including a plurality of levels, each of said levels containing local routing resources and a plurality of blocks, each of said blocks including either a module or another of said levels.
5. The interface architecture of claim 1 wherein said FPGA portion of said integrated circuit has a plurality of levels, each of said levels containing local routing resources and a plurality of blocks, each of said blocks including either a module or another of said levels; and said mask programmed dedicated interface tracks are connected between said modules or blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion.

6. The interface architecture of claim 5, wherein each of said blocks in said FPGA portion contains local routing resources.

5 7. The interface architecture of claim 5, further including an FPGA-ASIC routing channel arranged between said dedicated interface tracks and said ASIC portion.

10 8. The interface architecture of claim 3 or 7, wherein said FPGA-ASIC routing channel is mask-programmable.

15 9. The interface architecture of claim 3 or 7 wherein said FPGA-ASIC routing channel is field-programmable.

20 10. The interface architecture of claim 1 further including JTAG buffers arranged between said dedicated interface tracks and said ASIC portion.

25 11. The interface architecture of claim 1 or 9 further including a plurality of I/O modules arranged on the perimeter of the IC.

30 12. The interface architecture of claim 11, wherein one or more of said I/O modules are connected to said FPGA portion through a routing channel.

35 13. The interface architecture of claim 11, wherein one or more of said I/O modules are connected to said ASIC portion.

40 14. The interface architecture of claim 11 when dependent on claim 9, wherein one or more of said I/O modules are connected to said FPGA-ASIC routing channel.

45 15. The interface architecture of claim 1, wherein said ASIC portion is adjacent to one side of said FPGA portion.

50 16. The interface architecture of claim 1, wherein said ASIC portion is adjacent to two sides of said FPGA portion.

55 17. The interface architecture of claim 1, wherein said ASIC portion is adjacent to three sides of said FPGA portion.

18. The interface architecture of claim 1, wherein said ASIC portion is adjacent to four sides of said FPGA portion.

19. An integrated circuit having an interface architecture according to any one of the preceding claims.

20. A mask having a pattern representing at least a part

of a process layer usable to form an integrated circuit according to claim 19.

#### Patentansprüche

1. Schnittstellenarchitektur in einer integrierten Schaltung, welche umfasst:

- einen FPGA-Teil (14) der integrierten Schaltung mit Logikblöcken (20) für das Implementieren von logischen Funktionen und mit Verbindungskonnektoren für das programmierbare Verbinden der Logikblöcke;
- einen ASIC-Teil (12) der integrierten Schaltung mit maskenprogrammierten Logikschaltungen und maskenprogrammierten Verbindungsleitern zwischen den Logikschaltungen;
- maskenprogrammierte zugeordnete Schnittstellenspuren (24), welche zwischen den Logikblöcken in dem FPGA-Teil und den maskenprogrammierten Verbindungsleitern in dem ASIC-Teil angeschlossen sind; und
- Schnittstellenpuffer, welche in Reihe mit den zugeordneten Schnittstellenspuren zwischen dem FPGA-Teil und dem ASIC-Teil angeordnet sind;

**dadurch gekennzeichnet, dass:**

jeder der Schnittstellenpuffer umfasst:

- einen Eingangspuffer (32)
- einen Ausgangspuffer (30), wobei der Ausgangspuffer mit dem Eingangspuffer verbunden ist;
- drei Multiplexer, wobei zwei der Multiplexer (34-1, 34-2) mit dem Ausgangspuffer verbunden sind und einer der Multiplexer (34-3) mit dem Eingangspuffer verbunden ist; und
- ein konfigurierbares Register, einen konfigurierbaren Speicher oder ein konfigurierbares programmierbares Element (36), welcher bzw. welches mit jedem Satz Multiplexer verbunden ist.

2. Schnittstellenarchitektur nach Anspruch 1, **dadurch gekennzeichnet, dass** die Verbindungsleiter in dem FPGA-Teil lokale Routing-Ressourcen umfassen.

3. Schnittstellenarchitektur nach Anspruch 1, welche weiterhin einen zwischen den zugeordneten Schnittstellenspuren und dem ASIC-Teil angeordneten FPGA-ASIC-Routing-Kanal umfasst.

4. Schnittstellenarchitektur nach Anspruch 1, **dadurch gekennzeichnet, dass** der FPGA-Teil ein hierarchisches Design mit mehreren Ebenen aufweist, wobei jede der Ebenen lokale Routing-Ressourcen und mehrere Blöcke enthält, wobei jeder der Blöcke entweder ein Modul oder eine andere der Ebenen umfasst.

5. Schnittstellenarchitektur nach Anspruch 1, **dadurch gekennzeichnet, dass** der FPGA-Teil der integrierten Schaltung mehrere Ebenen aufweist, wobei jede der Ebenen lokale Routing-Ressourcen und mehrere Blöcke enthält, wobei jeder der Blöcke entweder ein Modul oder eine andere der Ebenen umfasst; und dass die maskenprogrammierten zugeordneten Schnittstellenspuren zwischen den Modulen oder Blöcken in dem FPGA-Teil und den maskenprogrammierten Verbindungsleitern in dem ASIC-Teil angeschlossen sind.

6. Schnittstellenarchitektur nach Anspruch 5, **dadurch gekennzeichnet, dass** jeder der Blöcke in dem FPGA-Teil lokale Routing-Ressourcen enthält.

7. Schnittstellenarchitektur nach Anspruch 5, welche weiterhin einen zwischen den zugeordneten Schnittstellenspuren und dem ASIC-Teil angeordneten FPGA-ASIC-Routingkanal umfasst.

8. Schnittstellenarchitektur nach Anspruch 3 oder 7, **dadurch gekennzeichnet, dass** der FPGA-ASIC-Routingkanal maskenprogrammierbar ist.

9. Schnittstellenarchitektur nach Anspruch 3 oder 7, **dadurch gekennzeichnet, dass** der FPGA-ASIC-Routingkanal feldprogrammierbar ist.

10. Schnittstellenarchitektur nach Anspruch 1, welche weiterhin zwischen den zugeordneten Schnittstellenspuren und dem ASIC-Teil angeordnete JTAG-Puffer umfasst.

11. Schnittstellenarchitektur nach Anspruch 1 oder 9, welche weiterhin mehrere am Umfang der IS angeordnete I/O-Module umfasst.

12. Schnittstellenarchitektur nach Anspruch 11, **dadurch gekennzeichnet, dass** eines oder mehrere der I/O-Module durch einen Routingkanal mit dem FPGA-Teil verbunden ist/sind.

13. Schnittstellenarchitektur nach Anspruch 11, **da-**

**durch gekennzeichnet, dass** eines oder mehrere der I/O-Module an dem ASIC-Teil angeschlossen ist/sind.

14. Schnittstellenarchitektur nach Anspruch 11 bei Abhängigkeit von Anspruch 9, **dadurch gekennzeichnet, dass** eines oder mehrere der I/O-Module an dem FPGA-ASIC-Routingkanal angeschlossen ist/sind.
15. Schnittstellenarchitektur nach Anspruch 1, **dadurch gekennzeichnet, dass** sich der ASIC-Teil angrenzend an einer Seite des FPGA-Teils befindet.
16. Schnittstellenarchitektur nach Anspruch 1, **dadurch gekennzeichnet, dass** sich der ASIC-Teil angrenzend an zwei Seiten des FPGA-Teils befindet.
17. Schnittstellenarchitektur nach Anspruch 1, **dadurch gekennzeichnet, dass** sich der ASIC-Teil angrenzend an drei Seiten des FPGA-Teils befindet.
18. Schnittstellenarchitektur nach Anspruch 1, **dadurch gekennzeichnet, dass** sich der ASIC-Teil angrenzend an vier Seiten des FPGA-Teils befindet.
19. Integrierte Schaltung mit einer Schnittstellenarchitektur nach einem der vorhergehenden Ansprüche.
20. Maske mit einem Muster, welches mindestens einen Teil einer Prozessschicht darstellt, welche zum Bilden einer integrierten Schaltung nach Anspruch 19 verwendbar ist.

#### Revendications

1. Architecture d'interface dans un circuit intégré, comprenant :
  - une partie FPGA (14) dudit circuit intégré ayant des blocs logiques (20) pour exécuter des fonctions logiques et des connecteurs d'interconnexion pour connecter de façon programmable lesdits blocs logiques ;
  - une partie ASIC (12) dudit circuit intégré ayant des circuits logiques programmés par masque et des conducteurs d'interconnexion programmés par masque entre lesdits circuits logiques ; des pistes d'interface dédiées programmées par masque (24) connectées entre lesdits blocs logiques dans ladite partie FPGA et lesdits conducteurs d'interconnexion programmés par masque dans ladite partie ASIC ; et

des tampons d'interface disposés en série avec lesdites pistes d'interface dédiées entre ladite partie FPGA et ladite partie ASIC ;

**caractérisée en ce que**  
chacun desdits tampons d'interface comprend :

un tampon d'entrée (32) ;  
un tampon de sortie (30), ledit tampon de sortie étant connecté au dit tampon d'entrée ;  
trois multiplexeurs, deux desdits multiplexeurs (34-1, 34-2) étant connectés au dit tampon de sortie et un desdits multiplexeurs (34-3) étant connecté au dit tampon d'entrée ; et  
un registre, une mémoire de stockage ou un élément programmable configurables (36) connecté à chaque jeu desdits multiplexeurs.

2. Architecture d'interface selon la revendication 1, dans laquelle les conducteurs d'interconnexion dans ladite partie FPGA comprennent des ressources de routage locales.
3. Architecture d'interface selon la revendication 1, comprenant en outre un canal de routage FPGA-ASIC disposé entre lesdites pistes d'interface dédiées et ladite partie ASIC.
4. Architecture d'interface selon la revendication 1, dans laquelle ladite partie FPGA a une structure hiérarchique comprenant une pluralité de niveaux, chacun desdits niveaux contenant des ressources de routage locales et une pluralité de blocs, chacun desdits blocs comprenant soit un module, soit un autre desdits niveaux.
5. Architecture d'interface selon la revendication 1, dans laquelle ladite partie FPGA dudit circuit intégré a une pluralité de niveaux, chacun desdits niveaux contenant des ressources de routage locales et une pluralité de blocs, chacun desdits blocs comprenant soit un module, soit un autre desdits niveaux ; et lesdites pistes d'interface dédiées programmées par masque sont connectées entre lesdits modules ou blocs dans ladite partie FPGA et lesdits conducteurs d'interconnexion programmés par masque dans ladite partie ASIC.
6. Architecture d'interface selon la revendication 5, dans laquelle chacun desdits blocs dans ladite partie FPGA contient des ressources de routage locales.
7. Architecture d'interface selon la revendication 5, comprenant en outre un canal de routage FPGA-ASIC disposé entre lesdites pistes d'interface dédiées et ladite partie ASIC.



8. Architecture d'interface selon la revendication 3 ou 7, dans laquelle ledit canal de routage FPGA-ASIC est programmable par masque.
9. Architecture d'interface selon la revendication 3 ou 7, dans laquelle ledit canal de routage FPGA-ASIC est programmable sur place. 5
10. Architecture d'interface selon la revendication 1, comprenant en outre des tampons JTAG disposés entre lesdites pistes d'interface dédiées et ladite partie ASIC. 10
11. Architecture d'interface selon la revendication 1 ou 9, comprenant en outre une pluralité de modules d'E/S disposés sur la périphérie du CI. 15
12. Architecture d'interface selon la revendication 11, dans laquelle un ou plusieurs desdits modules d'E/S sont connectés à ladite partie FPGA par un canal de routage. 20
13. Architecture d'interface selon la revendication 11, dans laquelle un ou plusieurs desdits modules d'E/S sont connectés à ladite partie ASIC. 25
14. Architecture d'interface selon la revendication 11 lorsqu'elle dépend de la revendication 9, dans laquelle un ou plusieurs desdits modules d'E/S sont connectés au dit canal de routage FPGA-ASIC. 30
15. Architecture d'interface selon la revendication 1, dans laquelle ladite partie ASIC est adjacente à un côté de ladite partie FPGA. 35
16. Architecture d'interface selon la revendication 1, dans laquelle ladite partie ASIC est adjacente à deux côtés de ladite partie FPGA.
17. Architecture d'interface selon la revendication 1, dans laquelle ladite partie ASIC est adjacente à trois côtés de ladite partie FPGA. 40
18. Architecture d'interface selon la revendication 1, dans laquelle ladite partie ASIC est adjacente à quatre côtés de ladite partie FPGA. 45
19. Circuit intégré ayant une architecture d'interface selon l'une quelconque des revendications précédentes. 50
20. Masque ayant un motif représentant au moins une partie d'une couche de procédé utilisable pour former un circuit intégré selon la revendication 19. 55

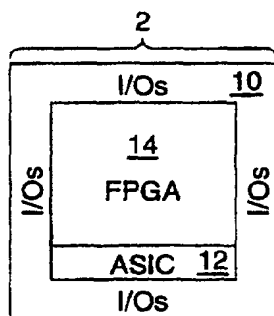


FIG. 1A

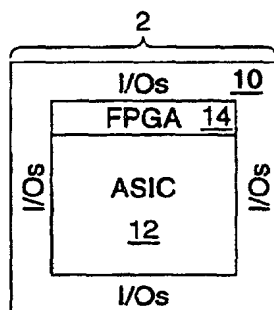


FIG. 1B

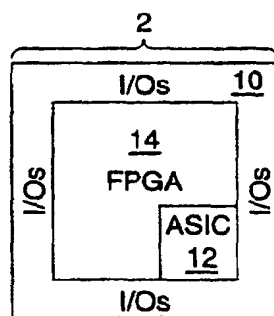


FIG. 1C

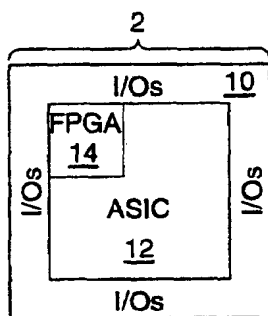


FIG. 1D

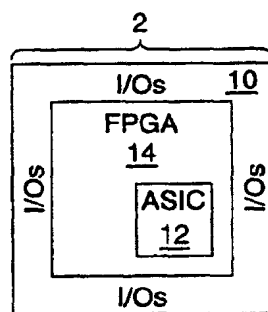


FIG. 1E

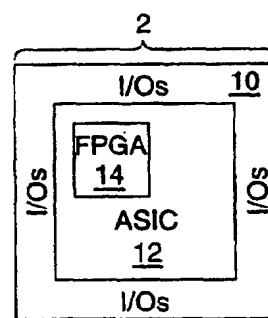


FIG. 1F

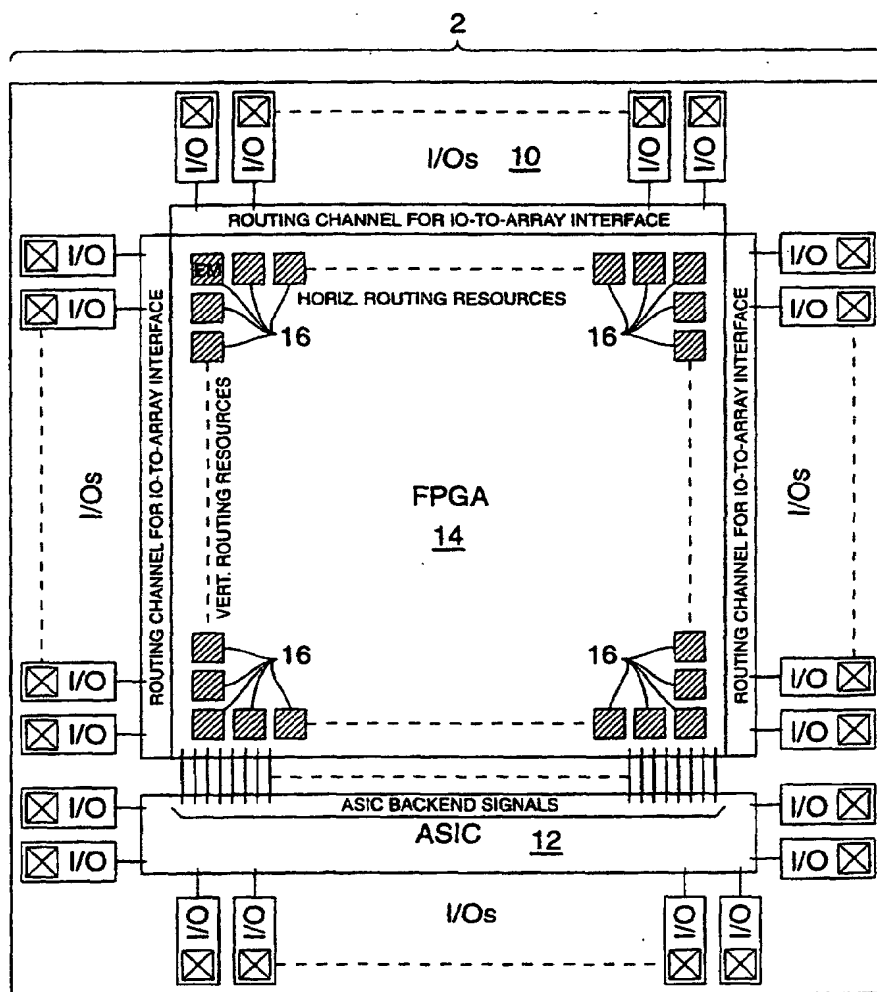


FIG. 2

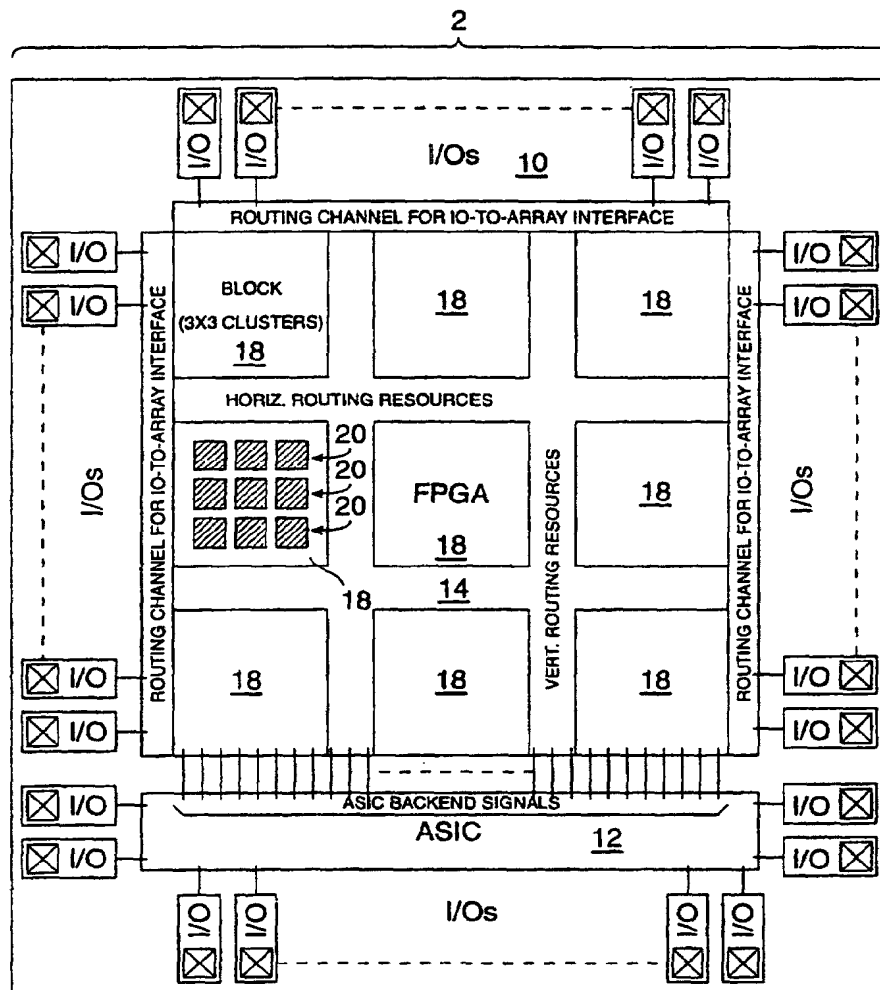
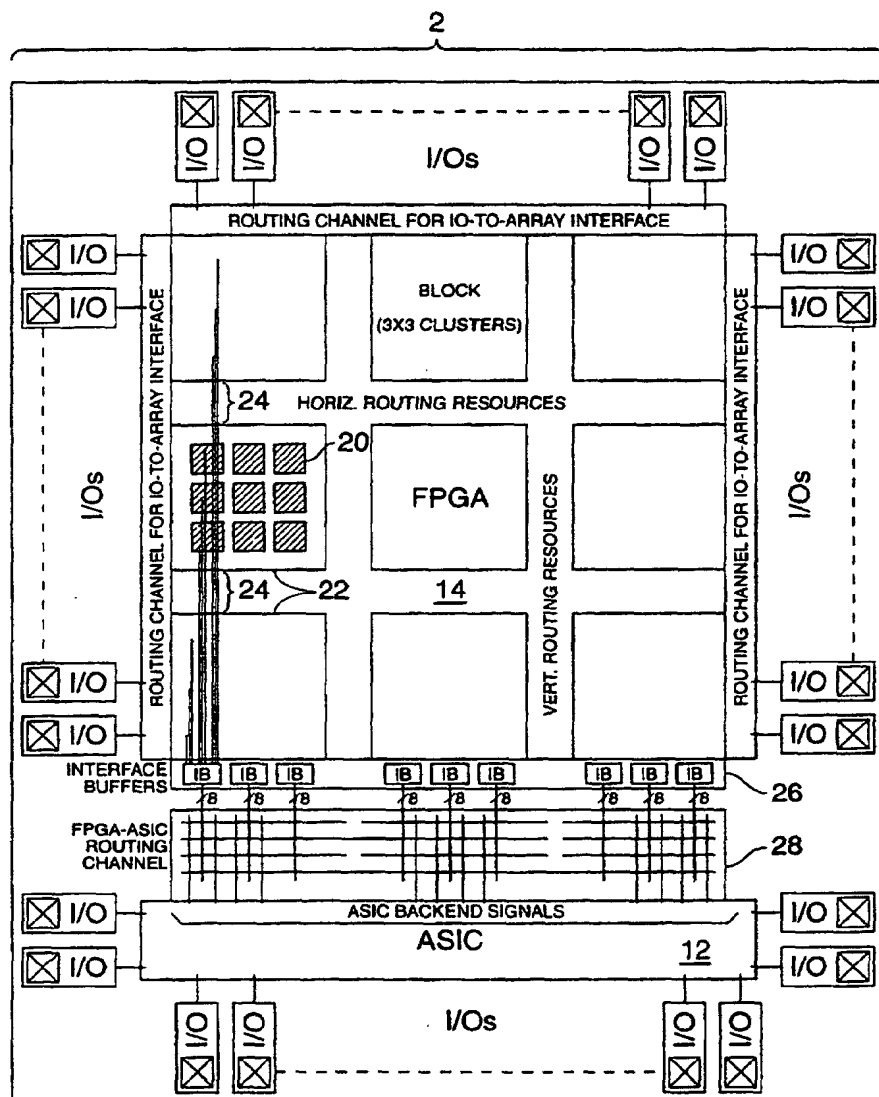


FIG. 3



**FIG. 4**

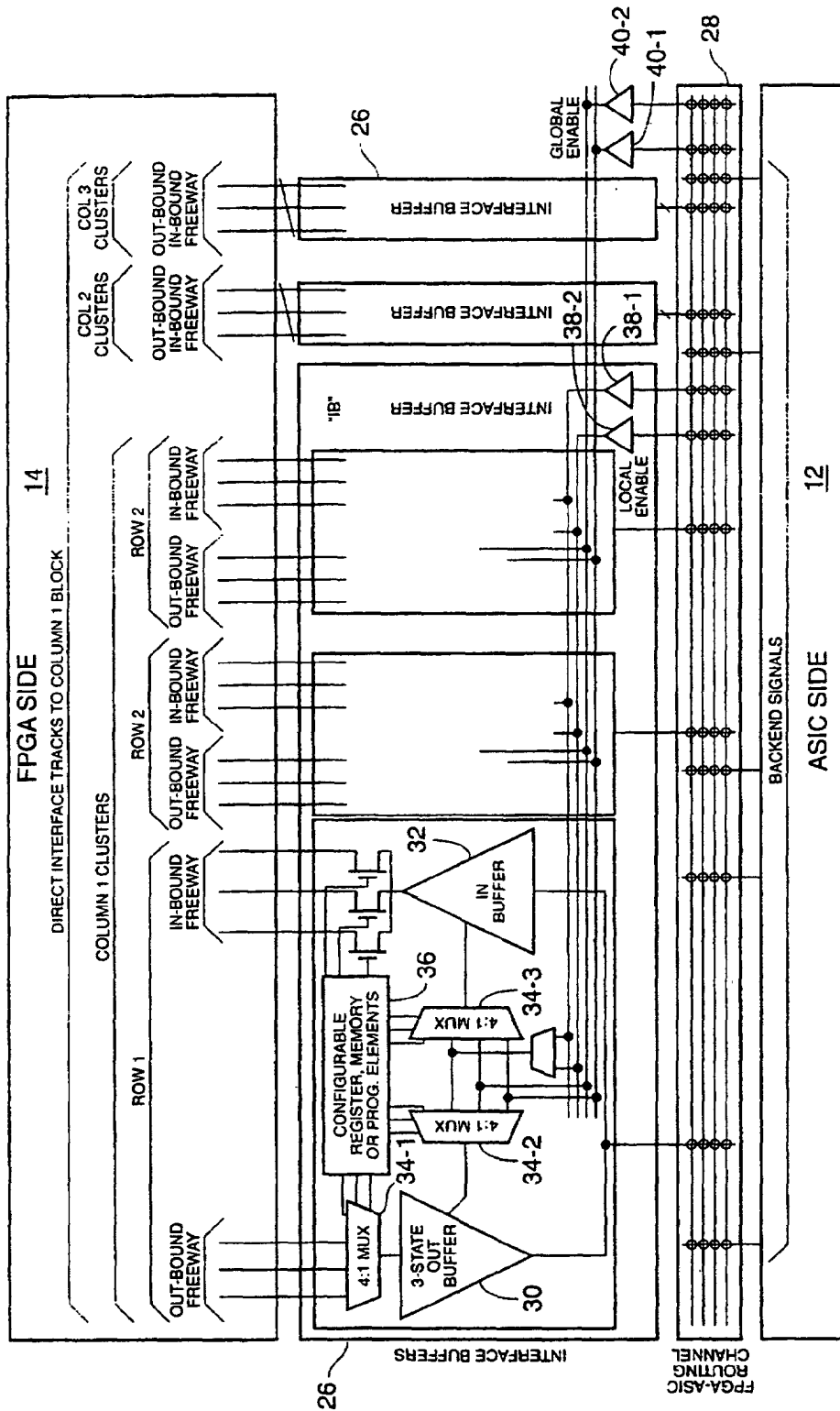


FIG. 5

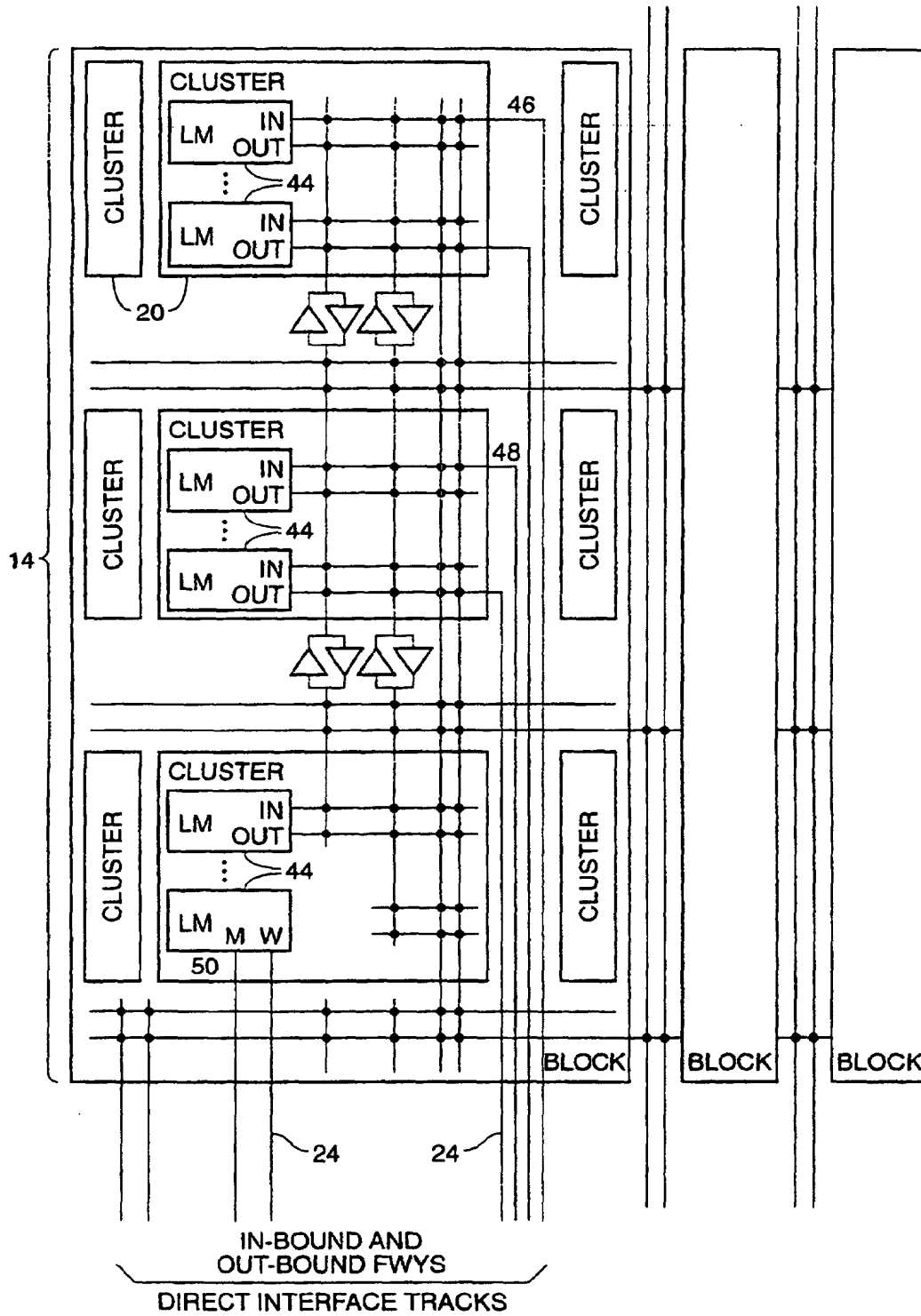


FIG. 6



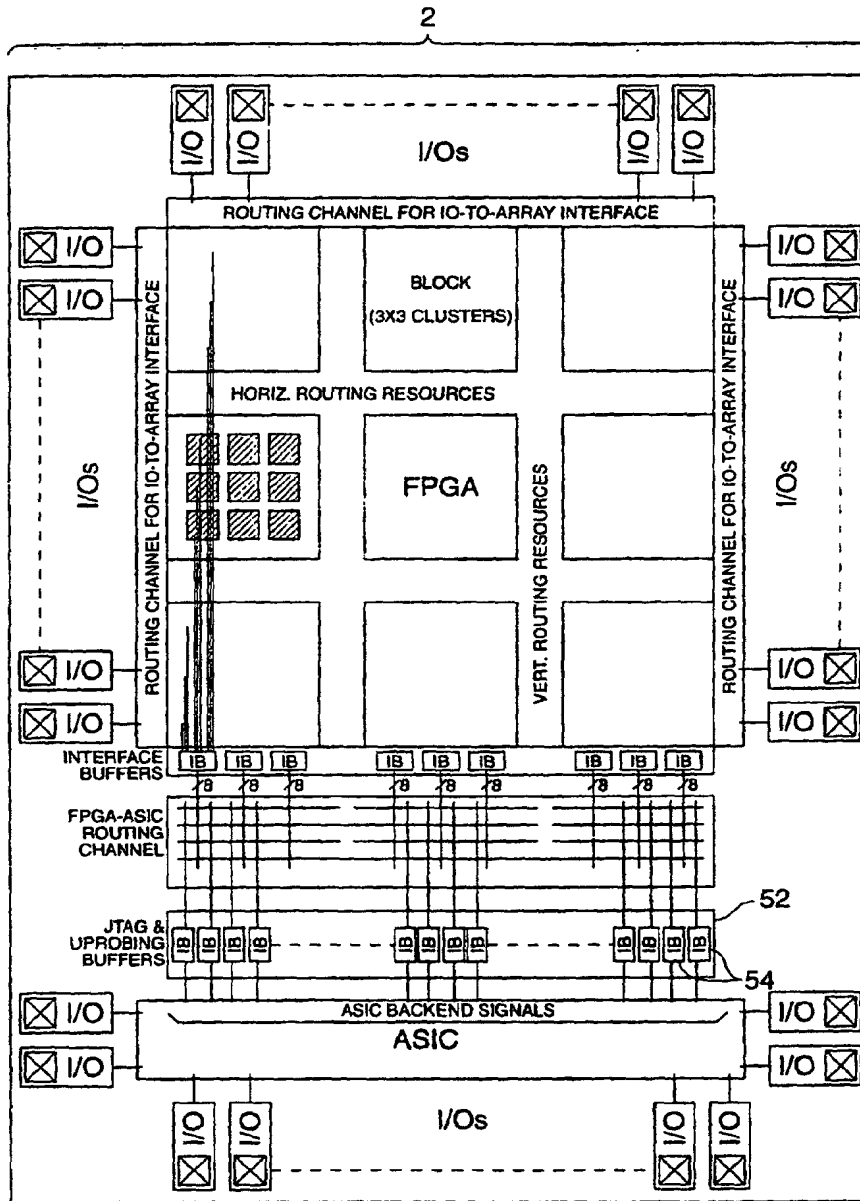


FIG. 7

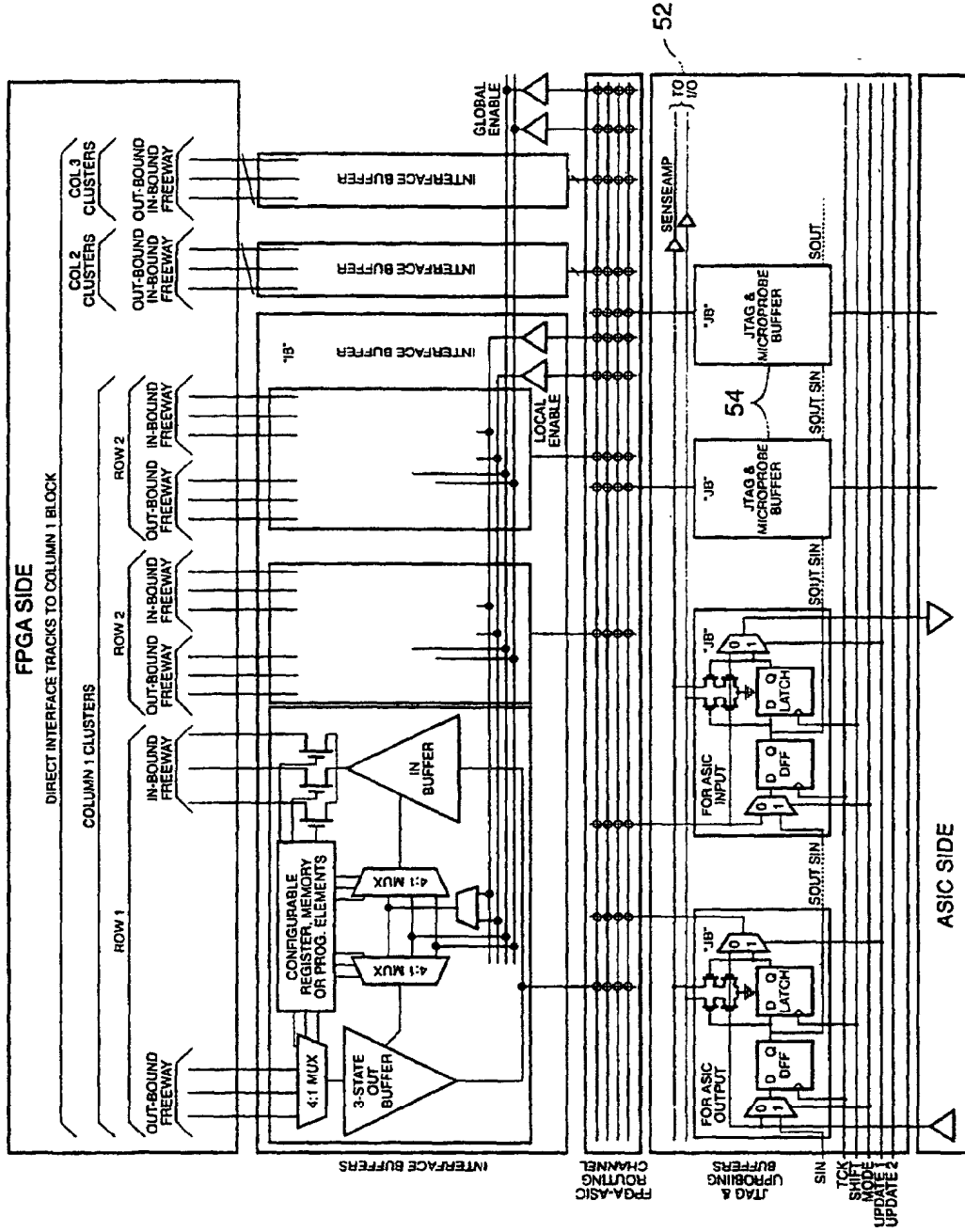


FIG. 8

2

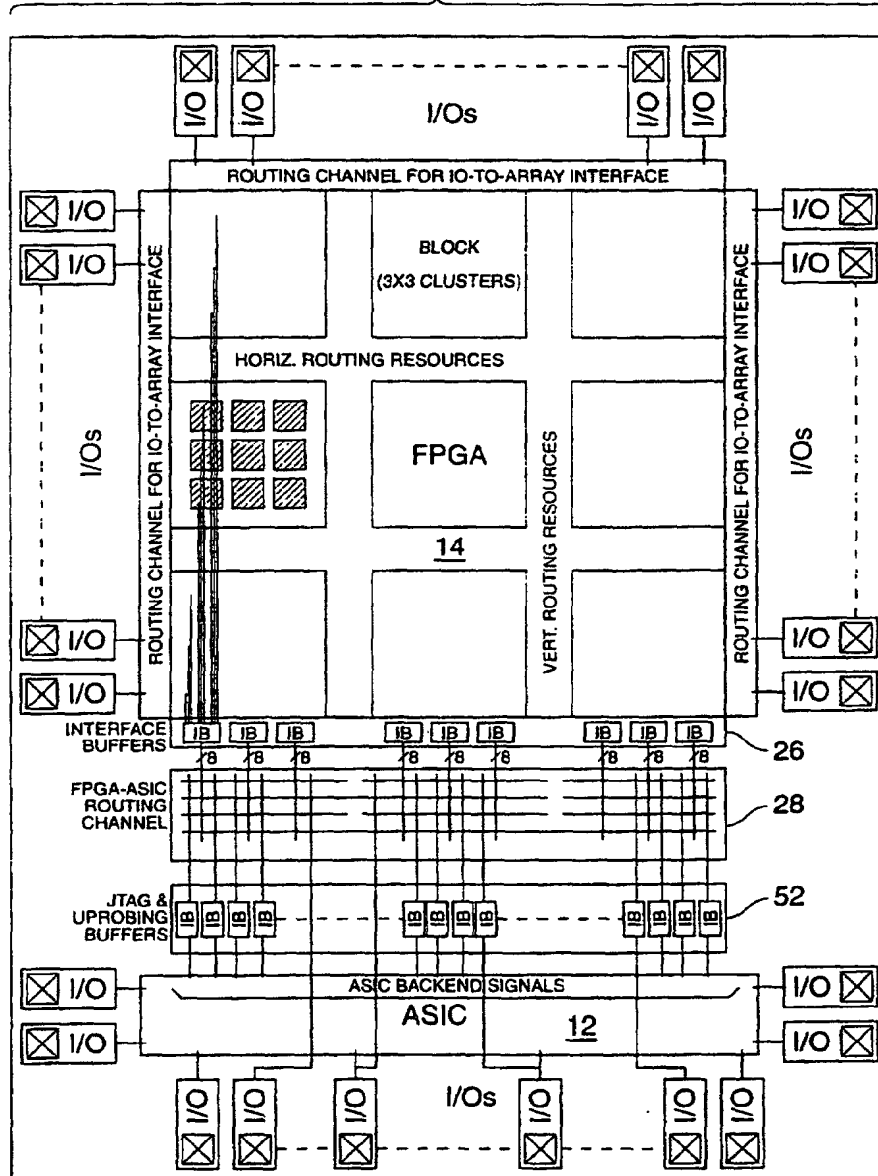


FIG. 9

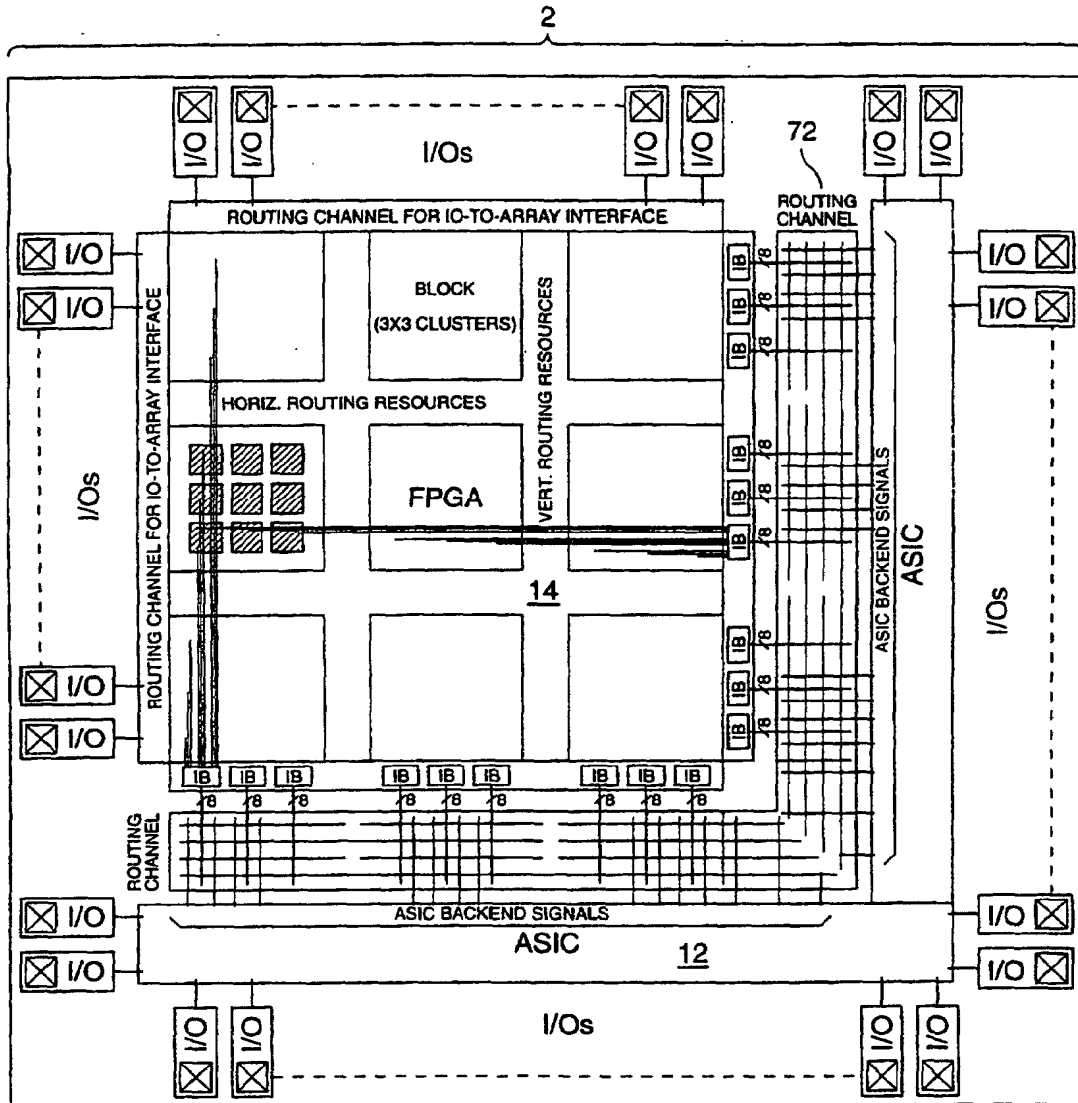


FIG. 10

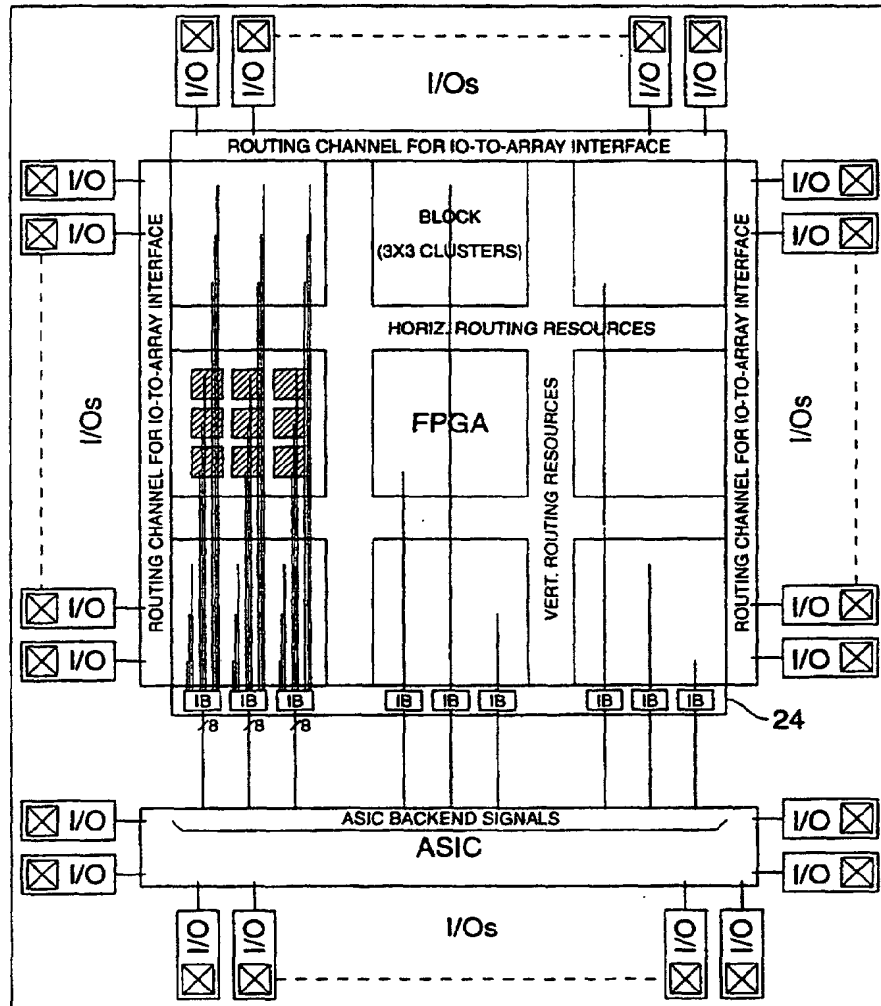


FIG. 11

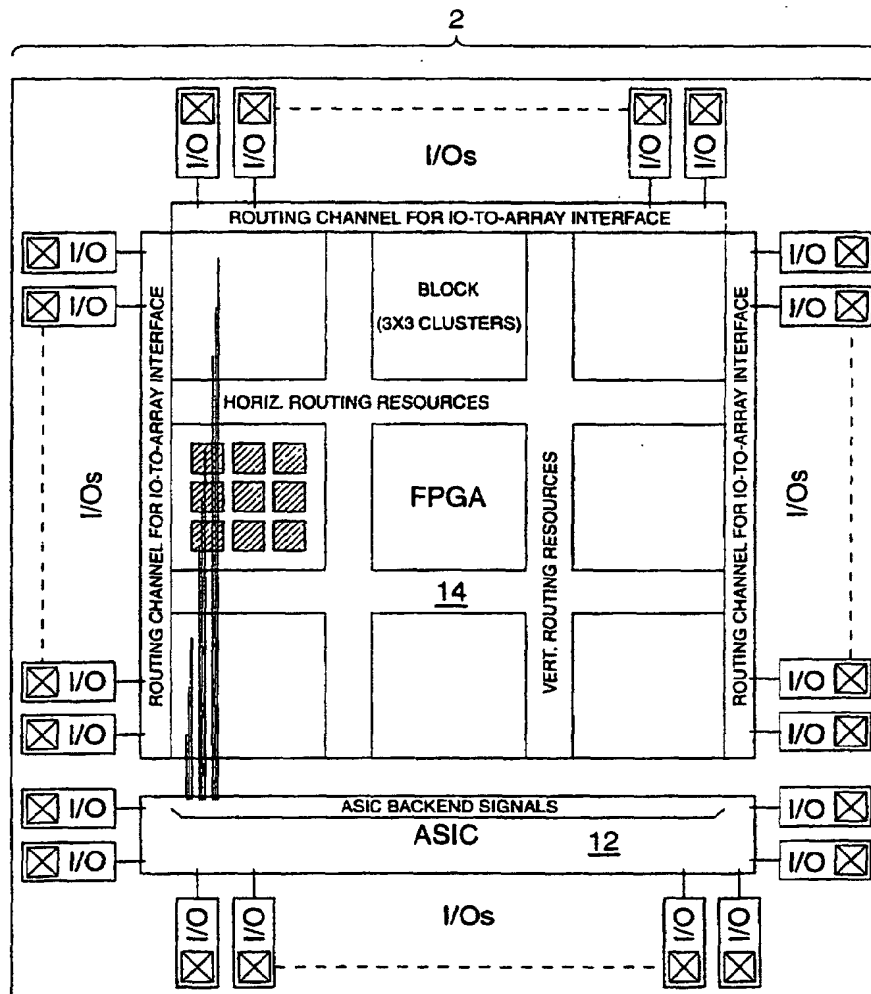


FIG. 12

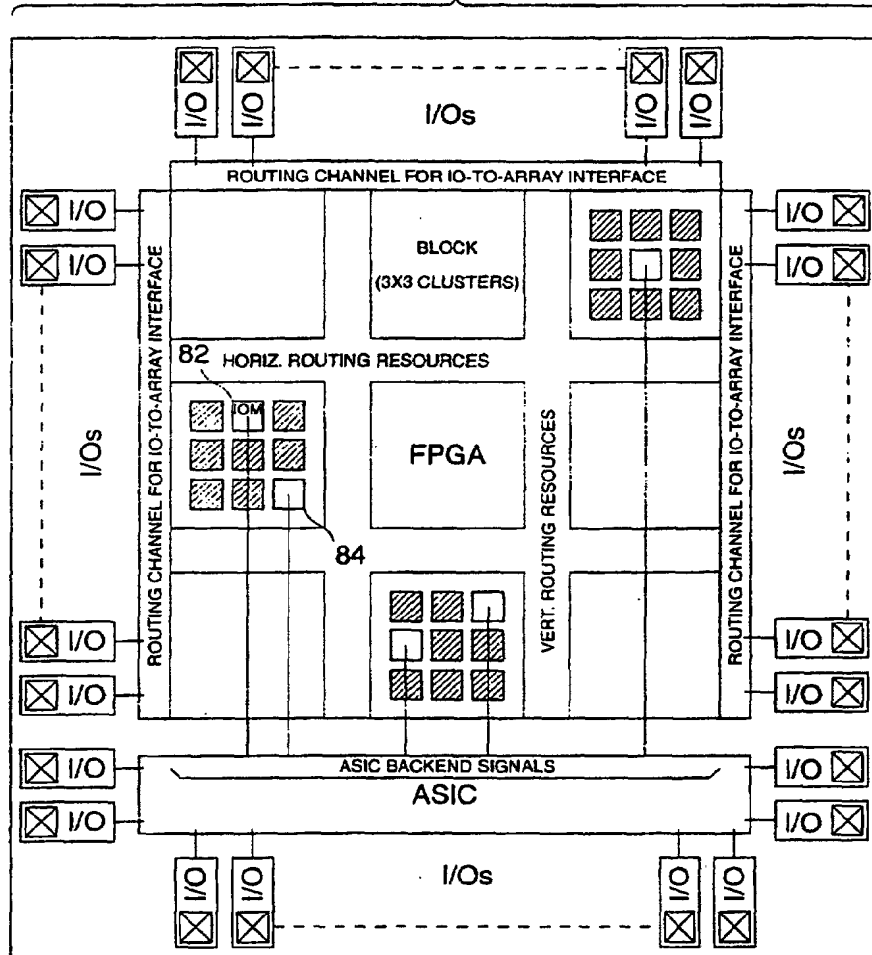


FIG. 13

2

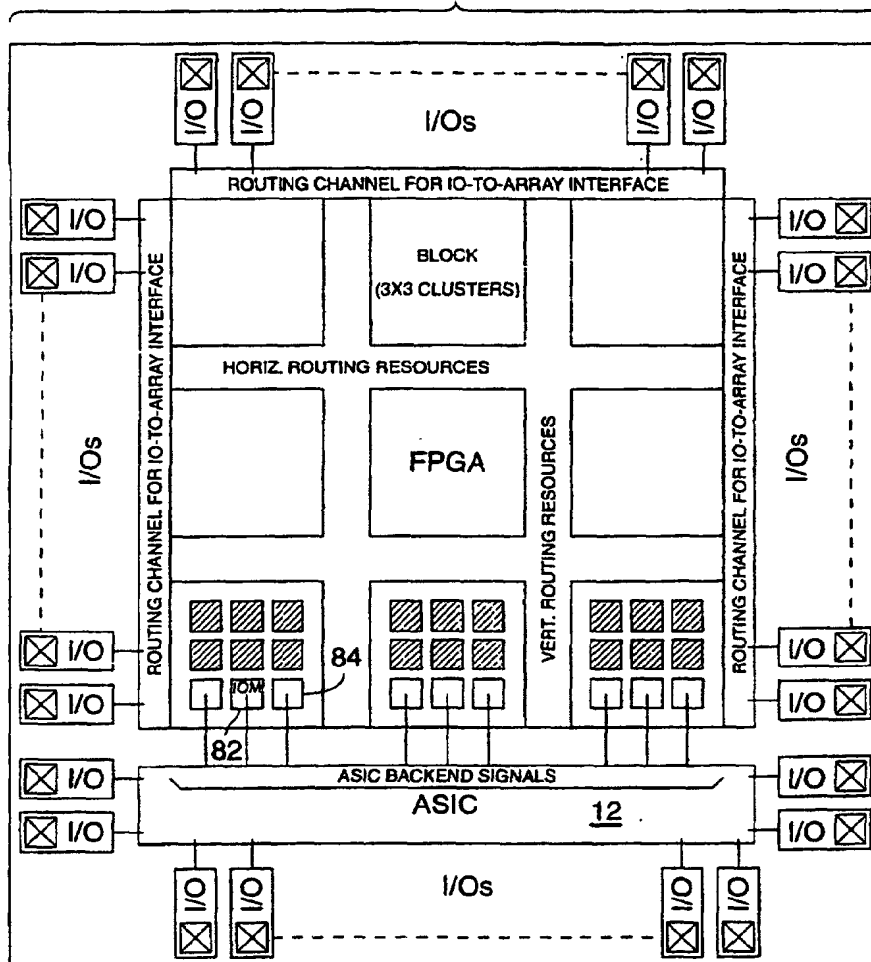


FIG. 14